

I CLAIM:

1. A CMOS analog multiplexer circuit comprising:  
multiple series n-channel/p-channel MOS transistor  
5 input switches;  
multiple series n-channel/p-channel MOS transistor  
output switches;  
multiple pull-down n-channel MOS transistor switches;  
wherein  
10 said circuit prevents cross-signal feed-through from  
unselected inputs by shunting said feed-through to  
circuit ground.
2. The CMOS analog multiplexer circuit of Claim 1  
15 further comprising:  
the input of a first series input n-channel/p-  
channel MOS transistor switch coupled to the first  
circuit input signal;  
the input of a second series input n-channel/p-  
20 channel MOS transistor switch coupled to the second  
circuit input signal;  
the input of a nth series input n-channel/p-channel  
MOS transistor switch coupled to the nth circuit  
input signal;  
25 the output of said first series input n-channel/p-  
channel MOS transistor switch coupled to the input

of a first output n-channel/p-channel MOS transistor switch and to the drain of a first n-channel MOS pull-down transistor;

the output of said second series input n-channel/p-channel MOS transistor switch coupled to the input of a second output n-channel/p-channel MOS transistor switch and to the drain of a second n-channel MOS pull-down transistor;

the output of said nth series input n-channel/p-channel MOS transistor switch coupled to the input of a nth output n-channel/p-channel MOS transistor switch and to the drain of a nth n-channel MOS pull-down transistor;

the outputs of said first, second, and nth output n-channel/p-channel MOS transistor switches coupled together and to circuit output;

the sources of said first, second, and nth n-channel MOS pull-down transistors coupled to circuit ground;

the gates of all said series input and output n-channel MOS transistor switches coupled to a logic control signal;

the gates of all said series input and output p-channel MOS transistor switches and all n-channel MOS pull-down transistors coupled to a logic control

signal which is the complement of said input/output transistor logic control signal.

3. The CMOS analog multiplexer circuit of Claim 2,  
5 further comprising MOS transistor layouts which have an even number of circuit fingers: wherein said MOS transistor's parasitic capacitance is reduced by more than 50%; and said MOS transistor's bandwidth is at least doubled.
- 10 4. The CMOS transistor layout of Claim 3 further comprising:  
a CMOS transistor whose architecture has the source and gate split in half such that it consists of the  
15 sequence: one-half source, one-half gate, drain, one-half gate, and one-half source;  
said CMOS transistor whose drain capacitance is half that of a conventional CMOS transistor;  
said CMOS transistor whose gate is split into two parts  
20 each having a width of  $w/2$ ;  
said CMOS transistor whose source is split into two parts each having a width of  $w/2$ ;  
said two gate parts coupled together and to transistor gate output;  
25 said two source parts coupled together and to transistor source output.

5. A CMOS analog multiplexer circuit comprising:  
multiple series n-channel MOS transistor input  
switches;  
5 multiple series n-channel MOS transistor output  
switches;  
multiple n-channel MOS transistor pull-down switches;  
wherein  
said circuit is capable of multiplexing small level  
10 analog signals having amplitudes which are a small  
fraction of the power source;  
said circuit's parasitic capacitance is reduced by as  
much as 50%;  
said circuit's bandwidth is at least doubled; and  
15 said circuit prevents cross-signal feed-through from  
unselected inputs by shunting said feed-through to  
circuit ground.

6. The CMOS analog multiplexer circuit of Claim 5  
20 further comprising:  
the input of a first series input n-channel MOS  
transistor switch coupled to the first circuit input  
signal;  
the input of a second series input n-channel MOS  
25 transistor switch coupled to the second circuit  
input signal;

the input of a nth series input n-channel MOS transistor switch coupled to the nth circuit input signal;

5 the output of said first series input n-channel MOS transistor switch coupled to the input of a first output n-channel transistor switch and to the drain of a first n-channel MOS pull-down transistor;

10 the output of said second series input n-channel MOS transistor switch coupled to the input of a second output n-channel MOS transistor switch and to the drain of a second n-channel MOS pull-down transistor;

15 the output of said nth series input n-channel MOS transistor switch coupled to the input of a nth output n-channel MOS transistor switch and to the drain of a nth n-channel MOS pull-down transistor; the outputs of said first, second, and nth output n-channel MOS transistor switches coupled together and to the circuit output;

20 the sources of said first, second, and nth n-channel MOS pull-down transistors coupled to circuit ground; the gates of all said series input and output n-channel MOS transistor switches coupled to a logic control signal;

the gates of all said n-channel MOS pull-down transistors coupled to a logic control signal which is the complement of said series input/output transistor logic control signal.

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7. A CMOS analog multiplexer circuit for use with differential input signals, comprising:

multiple positive and negative signal series n-channel MOS transistor input switches;

10 multiple positive and negative signal series n-channel MOS transistor output switches;

multiple positive and negative signal n-channel MOS transistor pull-down switches; wherein

said series positive and negative MOS transistor

15 switch's capacitance is reduced by at least 50% by means of eliminating the p-channel MOS transistors;

said circuit's bandwidth is at least doubled by means of eliminating said p-channel MOS transistors;

said circuit is capable of multiplexing small level

20 analog signals having amplitudes which are a small fraction of the power source; and

said circuit prevents cross-signal feed-through from unselected inputs by shunting said feed-through to circuit ground.

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8. The CMOS analog multiplexer circuit of Claim 7

further comprising:

the positive inputs of multiple differential input  
signals coupled to corresponding multiple positive

5 input series n-channel MOS transistor switches,  
respectively;

the outputs of said multiple positive input series  
input n-channel MOS transistor switches coupled to  
the inputs of multiple positive output n-channel MOS  
10 transistor switches, respectively, and to the drains  
of multiple positive n-channel MOS pull-down  
transistors;

the outputs of said multiple positive output  
n-channel MOS transistor switches coupled together  
15 and connected to the positive differential circuit  
output;

the sources of said multiple positive n-channel MOS  
pull-down transistors coupled to circuit ground;

the gates of all said positive series input and  
20 output n-channel MOS transistor switches coupled to  
a logic control signal;

the gates of all said positive n-channel MOS pull-  
down transistors coupled to a logic control signal  
that is complementary to said positive series  
25 input/output logic control signal;

the negative inputs of multiple differential input signals coupled to corresponding multiple negative input series n-channel MOS transistor switches, respectively;

5 the outputs of said multiple negative input series input n-channel MOS transistor switches coupled to the inputs of multiple negative output n-channel MOS transistor switches, respectively, and to the drains of multiple negative n-channel MOS pull-down

10 transistors;

the outputs of said multiple negative output n-channel MOS transistor switches coupled together and connected to the negative differential circuit output;

15 the sources of said multiple negative n-channel MOS pull-down transistors coupled to circuit ground; the gates of all said negative series input and output n-channel MOS transistor switches coupled to a logic control signal;

20 the gates of all said negative n-channel MOS pull-down transistors coupled to a logic control signal that is complementary to said negative series input/output logic control signal.



9. The CMOS analog multiplexer circuit of Claim 6 or 8 further comprising MOS transistor layouts having an even number of circuit fingers: wherein said MOS transistor's parasitic capacitance is further reduced by more than 50%; and said MOS transistor's bandwidth is further improved by at least two times.

10. The CMOS transistor layout of Claim 9 further comprising:  
a CMOS transistor whose architecture has the source and gate split in half such that it consists of the sequence: one-half source, one-half gate, drain, one-half gate, and one-half source;  
said CMOS transistor whose drain capacitance is half that of a conventional CMOS transistor;  
said CMOS transistor whose gate is split into two parts each having a width of  $w/2$ ;  
said CMOS transistor whose source is split into two parts each having a width of  $w/2$ ;  
said two gate parts coupled together and to transistor gate output;  
said two source parts coupled together and to transistor source output.

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